ABSTRACT

A semiconductor integrated device which comprises a memory cell 20 holding bit information; a pair of bit lines connected to the memory cell via which the bit information is input and output in predetermined cycles; and an output section 100 that latches an output from the memory cell via one bit line of the pair and the other bit line and outputs the bit information acquired from the one bit line as a result of reading from the memory cell, and which pre-charges the pair of bit lines before access to the memory cell. The memory cell 20 has a cutoff circuit (N24) that cuts off the other bit line to hold voltage thereof produced by pre-charging when the bit information held in the memory cell is read out.